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EXAMINER	
ODLAND, DAVID E	

ART UNIT	PAPER NUMBER
2662	12

DATE MAILED: 05/18/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/452,828	BUCKLAND ET AL.	
	Examiner	Art Unit	
	David Odland	2662	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *24 February 2004*.

2a)☒ This action is **FINAL**. 2b)☐ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-37* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) *1-37* is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☐ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☐ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date _____.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____.
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Response to Amendment

1. The following is a response to the amendments filed on 2/24/2004.

Claim Rejections - 35 USC § 102

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

3. Claims 1,2,4,5,7 and 9-12,16-18, 21-25,36 and 37 are rejected under 35 U.S.C. 102(e) as being anticipated by Koenig et al. (USPN 6,101,198), hereafter known as Koenig.

Referring to claims 1,2,4,5,7 and 9-11, Koenig discloses a time slot interchanger (TSI) for a telecommunications node (a TSI circuit (see figure 4 and claim 1)), comprising an exchange memory (the TSI comprises RAM (see column 11 lines 34-41)) comprising a plurality of exchange memory slots (RAM is divided into ODD input, EVEN input and OUTPUT buffer sections which can be considered 'slots' (see figures 4,10 and 15 and claim 1)), each exchange memory slot sized to store a traffic channel (the ODD and EVEN buffers each store frames of a highway signal which comprises 4 T1 signals (see figures 10 and 15 and claim 1)) and comprising a plurality of discretely addressable fields sized to store a sub-channel (the channels of the T1 signals are stored in entries of the input buffers which are discretely addressed because they are implemented with RAM (see figure 15 and claim 1)), and a controller operable in

response to predefined switching instructions (a DSP processor performs the TSI functions according to stored instructions (see figure 5 and claim 1)) to write a sub-channel received in a first channel to a first field in a memory slot (the DSP writes a T1 channel, which is a sub-channel of the highway signal, that is stored the EVEN input buffer to an entry of the OUTPUT buffer (see figure 15 and claim 14)) and to write a sub-channel received in a second channel to a second field in the memory slot (the DSP also writes T1 channels of other highway signals that are in the ODD input buffer to the OUTPUT buffer, thus performing TSI functions (see figures 5 and 15 and claim 14)), so that the sub-channel written to the first field and the sub-channel written to the second field may be read from the memory sot as a single traffic channel (the entries in the OUTPUT buffer are read out of the buffer as a new highway signal (see column 12 lines 41-67 and figure 10));

the controller further operable to read a first sub-channel from a memory slot to an egress time slot and a second sub-channel in the memory slot to a disparate egress time slot (the T1 channels are interchanged (i.e. time slot interchanged) and can read out of the buffer in an output frame such that the time slots from the ODD and EVEN input buffers are not read out of the OUTPUT buffer in the same frame (see figures 4,5,10 and 15 an claim 1 and 14));

the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in a memory slot (the T1 channel written to an entry of one of the ODD or EVEN input buffers can be written to an entry of the OUTPUT buffer (see figure 15 and claim 14));

the controller further operable to write a sub-channel in a field of a memory slot to a disparate field in an egress time slot (the T1 channel written to an entry of one of the ODD or

EVEN input buffers can be written to the OUPUT buffer which forms a frame that is transmitted during a time period (see figure 15 and claim 14));

the exchange memory comprising an exchange random access memory (RAM) (the DSP memory can be randomly accessed (see claims 1 and 3)) and an exchange register bank (an OUTPUT buffer (see figures 5 and 15 and claims 1 and 14)), the exchange RAM comprising a plurality of exchange RAM slots each sized to store the traffic channels (the DSP memory includes the ODD and EVEN input buffers and the OUTPUT buffer which can be considered slots and are sized to each store a frame comprising 4 T1 signals (see figures 4,5,10 and 15 and claims 1 and 14)) and comprising a plurality of discretely addressable fields sized to store a sub-channel (each of the buffers has entries which are used to store the channels of the T1 signals (see figure 15 and claim 14)) and the exchange register bank comprising a plurality of exchange registers each sized to store the traffic channel (the OUPUT buffer is sized to store a frame of data (see figure 15)) and comprising a plurality of discretely addressable fields sized to store a sub-channel (the OUPUT buffer also includes entries which are used to store the channels of the interchanged T1 signals (see figure 15));

the controller further operable to write a first sub-channel in an exchange RAM slot to a first exchange register (the DSP writes an entry of the EVEN input buffer to an entry in the OUPUT buffer (see figure 15 and claim 14)) and to write a second sub-channel in the exchange RAM slot to a second exchange register (the DSP then writes an entry in the ODD input buffer to the OUPUT buffer (see figure 15 and claim 14));

the controller further operable to write a sub-channel in a field of an exchange RAM slot to a disparate field in an exchange register (the DSP writes an entry from the EVEN input buffer

to the OUPUT buffer which is disparate from the ODD input buffer (see figure 15 and claim 14));

the exchange register is internal to the controller (the OUPUT buffer is inside and par tof the DSP (see figures 4 and 5)).

4. Referring to claims 12,16,17, 36 and 37, Koenig discloses a method for time division multiplex (TDM) switching of traffic in a telecommunications node (a TSI method (see abstract and figures 4 and 5)), comprising receiving a traffic stream comprising a plurality of traffic channels (a plurality of input signals are received as frames (see figure 10 and 15 and claim 1)) having discrete sub-channels (the frames comprise 4 T1 signals, which comprise 24 channels each (see figures 4 and 5)), writing a first traffic channel that includes a first sub-channel to a first memory slot in an exchange memory (a first highway which includes T1 sub-channels in written to the EVEN buffer, which as a whole can be considered a 'slot' of the RAM (see figured 10,11 and 15)), writing a second traffic channel that includes a second sub-channel to a second memory slot in an exchange memory (a second highway which also includes T1 sub-channels in written to the ODD buffer, which as a whole can be considered as another 'slot' of the RAM (see figured 10,11 and 15)), writing the first sub-channel to a first field in a third memory slot (a T1 channel of a highway signal in the EVEN input buffer is written to an entry of the OUTPUT buffer, which can be considered a memory 'slot' (see figure 15 and claims 1 and 14)), writing the second sub-channel to a second field in the third memory slot (a T1 channel of another highway signal in the ODD input buffer is written to an different entry of the OUPUT buffer (see figure 15 and claims 1 and 14)) and reading the sub-channels from the third memory slot to an egress

time slot as a single traffic channel (an interchanged frame is read from the OUTPUT buffer as a single serial output and transmitted during a time period (i.e. an egress time slot) (see figure 15 and claims 1 and 14)) (note, regarding claim 37, since Koenig performs Time Sot Interchange of the incoming highways, the outgoing highways can be considered as 'modified data', thus anticipated the claimed invention);

writing each traffic channel to a separate random access memory (RAM) slot in an exchange RAM (the DSP comprises memory that can be randomly accessed and frames are written to each of the ODD and EVEN input buffers (see figures 10 and 15 and claim 1)), writing a sub-channel in a first RAM slot to a first field in an exchange register of an exchange register bank (a T1 channel written in the EVEN input buffer is written to an entry of the OUTPUT buffer (see figure 15 and claims 1 and 14)) and writing a sub-channel in a second RAM slot to a second field in the exchange register (a T1 channel written in the ODD input buffer is written to another entry of the OUTPUT buffer (see figure 15 and claims 1 and 14));

the exchange register is internal to a controller writing the sub-channels from the RAM slot to the exchange register (the OUTPUT buffer is part of the memory of the DSP (see claim 1)).

5. Referring to claim 18, Koenig discloses switch card for a telecommunications node (time slot interchanger in an access bank (see item 20 in figure 4)), comprising a time slot interchanger (TSI) (a TSI DSP circuit (see item 26 in figure 4)), a switch interface operable to receive traffic from a plurality of line cards for the TSI and to transmit traffic from the TSI to the line cards (the mux and demux FPGA interfaces T1 traffic and the TSI (see item 34 of figure 4)), an instruction

register operable to provide predefined switching instructions to the TSI for routing traffic to and from the line cards (the DSP uses stored instructions to perform TSI operations (see claim 1)), an exchange register bank (an output buffer (see figure 10)), an exchange random access memory (RAM) (the DSP has memory, which can be randomly accessed, that comprise an two input buffers that are used for exchanging data (see figure 10 and claim 1)) and the TSI responsive to the predefined switching instructions from the instruction register to write traffic channels received from the switch interface into the exchange RAM (data frames are stored in the memory of the DSP (see figure 10 and 15)), to write a sub-channel of a first channel that is stored in a first slot of exchange RAM to a first field in an exchange register of the exchange register bank (a T1 channel of a T1 signal that is stored in a section (slot) of an EVEN input part of the DSP memory is written to an entry of the output buffer (see figures 10 and 15 and claim 14)) and to write a sub-channel in a second slot of exchange RAM to a second field in the exchange register (a T1 channel of a T1 signal that is stored in a section (slot) of an ODD input part of the DSP memory is written to an entry of the output buffer (see figures 10 and 15 and claim 14)), so that the sub-channel written to the first field and the sub-channel written to the second field may be read from the memory sot as a single traffic channel (the entries in the OUTPUT buffer are read out of the buffer as a new highway signal (see column 12 lines 41-67 and figure 10));

6. Referring to claims 21-25, Koenig discloses a method for processing traffic in a time slot interchanger (TSI) (processing traffic in a TSI circuit (see abstract)) comprising receiving a traffic stream comprising a plurality of traffic channels (a data stream in received and stored as frames in ODD and EVEN input buffers (see figures 4 and 5 and 15 and claims 1 and 14)),

writing each traffic channel to a memory slot in an exchange memory (each frame is written to either the IDD ort EVEN input buffers, which are part of the memory of a DSP (see figures 4 and 15 and claim 1)), reading a traffic channel stored in a memory slot (a T1 channel stored in the EVEN buffer is read and sent to an OUPUT buffer (see figure 15)), modifying data to generate a modified traffic channel (the time slots of the T1 signals that comprise each frame stored in the ODD and EVEN buffers are interchanged (modified) and a newly interchanged frame is output from the OUPUT buffer (see figure 15 and claim 14)) and writing the modified traffic channel to a memory slot (the interchanged channels are written in the OUPUT buffer (see figure 15 and claim 14));

modifying the data based on logic operations provided with an instruction word for the TSI (the TSI functions are performed by a DSP through the use of stored instructions (see claim 1));

writing the modified traffic channel to a disparate traffic channel (the channels of the T1 signals of the input frames are interchanged and rewritten to a frame which is output from the OUTPUT buffer (see figure 15 and claim 14));

determining a value of the data in the traffic channel and performing a specified action when the data has a specified value (a connection array is used in combination with the instructions to the DSP such that certain T1 channels of the frames are interchanged with others depending on the values of the time slots the channels occupy in the T1 signal and with highway or T1 signal, out of the 4 T1 signals of the frame, they correspond to (see figure 11)).

merging data of the traffic channel with data from a disparate traffic channel to form a conference traffic channel (T1 channels form the frame in the EVEN input buffer are

interchanged with T1 channels from the ODD input buffer to form a combined output frame that in stored in the OUPUT buffer (see figure 15 and claim 14)).

Claim Rejections - 35 USC § 103

7. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

8. Claims 3,8,13,14,27 and 28 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig in view of Khacherian (USPN 5,768,257), hereafter referred to as Khacherian.

Referring to claims 3,8,13,14,27 and 28, Koenig discloses the system discussed above. Koenig does not disclose that system comprises more than two disparate input buffers and more than one disparate output buffer such that the operations of the claimed limitations could be performed (note, these limitations merely recite operations similar to that of their parent claims except that they use multiple and disparate memories). However, Khacherian discloses a network switching apparatus that includes a plurality of disparate inputs and a plurality of disparate outputs for processing data (se claims 1 and 5). It would have been obvious to one skilled in the art at the time of the invention to configure and implement the Koenig system with more disparate input buffers and plural disparate output buffers, as taught in Khacherian, because if one buffer was to fail other buffers would be available to compensate, thereby making Koenig more reliable. Furthermore, the buffers of Koenig are implemented such that they store only one frame each, thus causing a system bottleneck. Having more of these buffers would improve the

speed and throughput of the Koenig system thus reducing this bottleneck. Furthermore, the Koenig TSI circuit interchanges voice data that has a required level of quality that is to be maintained in order to be properly transported, received and listened to at a receiving node of the network. Therefore, system reliability, throughput and speed of the TSI circuit are particularly important in Koenig. Lastly, Koenig points out, in column 12 lines 23-25, that the TSI circuit could be implemented with any number of input and output buffers, thus strongly suggesting compatibility of the Koenig system with more buffers than that which are exemplified in the drawings and claims.

9. Claims 19,20,26,30 and 31-35 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig.

Referring to claims 26,30 and 31-35, Koenig discloses all the limitations recited in these claims, as pointed out in the above corresponding 35 U.S.C. 102(e) rejections of claims 12,16 and 21-15, respectively. However, Koenig does not disclose that the system is implemented in software stored on a computer readable medium. It would have been obvious to one skilled in the art at the time of the invention to implement the Koenig system in this manner because the developmental costs of a software implementation are less than that of a hardware based implementation. Furthermore, software is easier to upgrade than hardware.

Referring to claim 19, Koenig discloses the system discussed above. Koenig does not disclose writing a first sub-channel of a third channel that is stored in a third slot of the exchange RAM to a second exchange register associated with a fourth channel and to write a second sub-channel of the third channel to a third exchange register associated with a fifth channel.

However, It would have been obvious to one skilled in the art at the time of the invention to implement this feature into the Koenig system because doing so would make Koenig more flexible in that it can accommodate more channels and registers and thus provide the TSI function to more users.

Referring to claim 20, Koenig discloses the system discussed above. Furthermore, Koenig discloses that the exchange register is internal to the TSI (the output register is part of the memory of the DSP (see claim 1)).

10. Claims 6,15 and 29 are rejected under 35 U.S.C. 103(a) as being unpatentable over Koenig in view of Willie (USPN 5,883,902), hereafter referred to as Willie.

Referring to claims 6,15 and 29, Koenig discloses the system discussed above. Koenig does not disclose that the traffic channel is a DS-0 and the sub-channel is a 1/4 DS-0. However, Willie discloses a system wherein, ¼ DSO channels of a DSO are time slot interchanged (see column 2 lines 33-53). It would have been obvious to one skilled in the art at the time of the invention to implement this configuration is the Koenig system because such a configuration can be used to support ISDN services, as pointed out by Willie in column 2 lines 33-53. Therefore, this configuration would make Koenig more versatile and flexible by allowing the system to process data that uses the ISDN protocol and support users of the ISDN.

Response to Arguments

11. Applicant's arguments filed 02/24/2004 have been fully considered but they are not persuasive.

On pages 16 last paragraph and page 18 first paragraph, the Applicant contends that Koenig fails to teach the claimed invention because Koenig does not disclose reading the sub-channels from the memory slot as a single traffic channel. The Examiner respectfully disagrees. Koenig clearly shows that a single signal is read out from the output buffer in a serial stream (see item 28 in figure 9).

On page 19 first paragraph regarding claim 21, the Applicant contends that Koenig does not teach of 'modifying data'. The Examiner respectfully disagrees. Koenig performs a Time Slot Interchange (TSI) function wherein data contained in an incoming signal's time slots are time and space switched such that the outgoing signal is different due to the data in the time slots being rearranged and therefore this outgoing data can be considered a 'modified' version of the input data. There are no limitations that would distinguish the claimed 'data modification' from the 'data modification' being performed in Koenig.

On page 21, the Applicant argues that the combination of Koenig in view of Khacherian is improper because Khacherian does not disclose any writing of sub-channels. The Examiner respectfully disagrees. This limitation is disclosed by the primary reference, Koenig, and therefore the combination is proper.

Conclusion

12. Applicant's amendment necessitated any new ground(s) of rejection presented in this Office action. Accordingly, **THIS ACTION IS MADE FINAL**. See MPEP § 706.07(a). Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to David Odland, who can be reached at (703) 305-3231 on Monday – Friday during the hours of 8am to 5pm.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Hassan Kizou, can be reached at (703) 305-4744. The fax number for the organization where this application or proceeding is assigned is (703) 872-9306.

Any inquiry of a general nature or relating to the status of this application or proceeding should be directed to the receptionist, who can be reached at (703) 305-4750.

deo

May 16, 2004

JOHN PEZZLO
PRIMARY EXAMINER